WHAT IS CLAIMED IS:

1. A method for reducing the slew rate of transition edges of a digital signal on a node of an integrated circuit, comprising:

connecting a first switchably conductive device characterized by a first threshold voltage between said node and a voltage source, said first switchably conductive device responsive to a first input signal to allow current conduction from said voltage source to said node when said first input signal is offset from said voltage source by a voltage substantially equal to or greater than said first threshold voltage and to disallow said current conduction when said first input signal is offset from said voltage source by a voltage less than said first threshold voltage;

connecting a second switchably conductive device characterized by a second threshold voltage greater than said first threshold voltage between said node and said voltage source, said second switchably conductive device responsive to a second input signal to allow current conduction from said voltage source to said node when said second input signal is offset from said voltage source by a voltage substantially equal to or greater than said second threshold voltage and to disallow said current conduction when said second input signal is offset from said voltage source by a voltage less than said second threshold voltage; and

connecting a driving signal as said first input signal of said first switchably conductive device and as said second input signal of said second switchably conductive device.

2. A method in accordance with claim 1, comprising:

connecting between said node and said voltage source one or more additional switchably conductive devices each characterized by a respective threshold voltage different than said first threshold voltage, said second threshold voltage, and each other respective threshold voltage, each said one or more additional switchably conductive devices responsive to a respective input signal to allow current conduction from said voltage source to said node when said respective input signal is offset from said voltage

source by a voltage substantially equal to or greater than said respective threshold voltage and to disallow said current conduction when said respective input signal is offset from said voltage source by a voltage less than said respective threshold voltage; and

connecting said driving signal as said respective input signal of said respective switch of each of said respective one or more additional switchably conductive devices.

3. An apparatus for reducing the slew rate of transition edges of a digital signal on a node of an integrated circuit, comprising:

a first switchably conductive device characterized by a first threshold voltage, said first switchably conductive device connected between said node and a voltage source and responsive to a driving signal to allow current conduction from said voltage source to said node when said driving signal is offset from said voltage source by a voltage substantially equal to or greater than said first threshold voltage and to disallow said current conduction when said driving signal is offset from said voltage source by a voltage less than said first threshold voltage; and

a second switchably conductive device characterized by a second threshold voltage greater than said first threshold voltage, said second switchably conductive device connected between said node and said voltage source and responsive to said driving signal to allow current conduction from said voltage source to said node when said driving signal is offset from said voltage source by a voltage substantially equal to or greater than said second threshold voltage and to disallow said current conduction when said driving signal is offset from said voltage source by a voltage less than said second threshold voltage.

4. An apparatus in accordance with claim 3, wherein said first switchably conductive device and said second switchably conductive device comprise field effect transistors (FETs).

5. An apparatus in accordance with claim 3, comprising:

one or more additional switchably conductive devices each characterized by a respective threshold voltage different than said first threshold voltage, said second threshold voltage, and each other respective threshold voltage, each said one or more additional switchably conductive devices connected between said node and said voltage source and responsive to said driving signal to allow current conduction from said voltage source to said node when said driving signal is offset from said voltage source by a voltage substantially equal to or greater than said respective threshold voltage and to disallow said current conduction when said driving signal is offset from said voltage source by a voltage less than said respective threshold voltage.

6. An apparatus in accordance with claim 3, wherein said first switchably conductive device, said second switchably conductive device, and said one or more additional switchably conductive devices each comprise field effect transistors (FETs).

7. A method for controlling the slew rate of transition edges of a digital signal on a node of an integrated circuit, said method comprising the steps of:

driving, with a driving signal, a first switchably conductive device characterized by a first threshold voltage and connected between said node and a voltage source, said first switchably conductive device responsive to said driving signal to allow current conduction from said voltage source to said node when said driving signal is offset from said voltage source by a voltage substantially equal to or greater than said first threshold voltage and to disallow said current conduction when said driving signal is offset from said voltage source by a voltage less than said first threshold voltage;

driving, with said driving signal, a second switchably conductive device characterized by a second threshold voltage greater than said first threshold voltage an connected between said node and said voltage source, said second switchably conductive device responsive to said driving signal to allow current conduction from said voltage source to said node when said

driving signal is offset from said voltage source by a voltage substantially equal to or greater than said second threshold voltage and to disallow said current conduction when said driving signal is offset from said voltage source by a voltage less than said second threshold voltage.

8. A method for controlling the slew rate of transition edges of a digital signal on a node of an integrated circuit, said method comprising the steps of:

monitoring a level of a driving voltage;

when said level reaches a first threshold voltage, stepping up conduction of current to said node;

when said level reaches a next predefined threshold voltage, stepping up conduction of current to said node.

9. A method in accordance with claim 8, comprising:

repeating said second stepping up step for one or more additional next predefined threshold voltages.

10. A method for controlling the slew rate of transition edges of a digital signal on a node of an integrated circuit, said method comprising the steps of:

monitoring a level of a driving voltage;

when said level reaches a first threshold voltage, stepping down conduction of current to said node;

when said level reaches a next predefined threshold voltage, stepping down conduction of current to said node.

11. A method in accordance with claim 10, comprising:

repeating said second stepping down step for one or more additional next predefined threshold voltages.